Agenda

Optimize Your Code for the Intel XEON PHI
April 5, 2013

PART I - Introduction (1.5 hours) - Lars Koesterke 8:30-10:00

- Xeon Phi Architecture
- Programming models
    - Native Execution (MPI / Threads / MPI+Threads)
    - MPI on host and Phi
    - MPI on host, offload to Phi
        - Targeted
        - Automatic (MKL)
    - Offload to host from the Phi

LAB

- Login and explore busybox

BREAK 10:00 -10:30

PART II - Native Execution (1.5 hours) – Luke Wilson 10:30 - noon

- Native Execution
    - Why run native?
    - How to build a native application?
    - How to run a native application?
    - Best practices for running native
        - KMP_AFFINITY
    - Optimization
        - Cache + ALU/SIMD details
        - Vectorization
        - Parallelization
        - Alignment
        - Compiler reports

LAB

- Interactive exercise using compiler reports
- Interactive exercise to show logical to physical proc mapping

LUNCH 12:00 - 1:00

PART III - Symmetric Execution (1.5 hours) – John Cazes 1:00 – 2:30

- MPI execution
    - Symmetric execution
        - Workload distribution
        - ibrun.sym
        - Correct pinning of MPI tasks on host and coprocessor
        - Interactive exercise showing symmetric at work
    - MPI + offload
    - Pinning tasks to host and MIC

LAB

- Exercise with symmetric execution and pinning

BREAK 2:30 - 3:00

PART IV - Offload Execution (2 hours hours) – Kent Milfeld - 3:00 - 5:00

- Offload to Phi
    - What is offloading?
    - Directives
    - Automatic offloading with MKL
    - Compiler assisted offloading
    - Offloading inside a parallel region

LAB

- Interactive exercise with simple offload and data transfer